PCB Layout and Design Guide for CH7038/9

Multi-Standard Display Interface Converter with Scaler

1.0 INTRODUCTION

The CH7038/9 is specifically designed for PC markets and consumer electronics devices which multiple high definition content display formats inputs/outputs are required. Built in with multi sophisticated timing receivers, the advanced video encoder, the flexible scaling engine and easy-to-configure audio interfaces, the CH7038/9 can drive LCD panel through either a single/dual channel LVDS/TTL interface or a 1/2 lane Display Port interface, and simultaneously output different display standards such as the HDMI/DVI or the analog YPbPr/RGB (VGA)/CVBS/S-Video. This device will help manufactures to reduce the cost of design, accelerate their time-to-market and expands products display capability to satisfy the user's experience.

This application note focuses only on the basic PCB layout and design guidelines for CH7038/9. Guidelines in component placement, power supply decoupling, grounding, input /output signal interface are discussed in this document.

The discussion and figures that follow reflect and describe connections based on the 176-pin LQFP package of the CH7038/9. Please refer to the CH7038/9 datasheet for the details of the pin assignments.

2.0 COMPONENT PLACEMENT AND DESIGN CONSIDERATIONS

Components associated with the CH7038/9 should be placed as close as possible to the respective pins. The following discussion will describe guidelines on how to connect critical pins, as well as describe the guidelines for the placement and layout of components associated with these pins.

2.1 Power Supply Decoupling

The optimum power supply decoupling is accomplished by placing a 0.1µF ceramic capacitor to each of the power supply pins as shown in **Figure 1**. These 0.1µF capacitors should be connected as close as possible to their respective power and ground pins using short and wide traces to minimize lead inductance. Whenever possible, a physical connecting trace should connect the ground pins of the decoupling capacitors to the CH7038/9 ground pins, in addition to ground vias.

2.1.1 Ground Pins

The analog and digital grounds of the CH7038/9 should be connected to a common ground plane to provide a low impedance return path for the supply currents. Whenever possible, each of the CH7038/9 ground pins should be connected to its respective decoupling capacitor ground lead directly, then connected to the ground plane through a ground via. Short and wide traces should be used to minimize the lead inductance. Refer to **Table 1** for the Ground pins assignment.

2.1.2 Power Supply Pins

Refer to **Table 1** for the Power supply pins assignment. Refer to **Figure 1** for Power Supply Decoupling.

Table 1: Power Supply Pins Assignment of the CH7038/9

Pin Assignment	# of Pins	Type	Symbol	Description
12, 38, 97, 133	4	Power	AVCC_33	Analog 3.3V Power Supply (3.3V)
23	1	Power	AVCC_HMRX	HDMI RX Power supply (3.3V)

119, 123	2	Power	AVCC_DAC	DAC Power supply (3.3V)
65, 69	2	Power	AVCC_LDTX	LVDS TX Power supply (3.3V) TTL TX Power supply (3.3V or 1.8V)
142, 170	2	Power	AVCC_LDRX	LVDS RX Power supply (3.3V) TTL RX Power supply (3.3V or 1.8V)
14, 27, 66, 109, 110	5	Power	DVDD	Digital 1.2V Power supply (1.2V)
49, 85, 129	3	Power	AVCC_12	Analog 1.2V Power supply (1.2V)
37	1	Power	AVCC_DPPLL_1V2	DP TX Power supply (1.2V)
111, 117	2	Power	AVCC_DPRX_1V2	DP RX Power supply (1.2V)
32,33	2	Power	AVDD_DPTX_1V2	DP TX Power supply(1.2V)
15,26	2	Power	AVDD_HMRX_1V2	HDMI RX Power supply(1.2V)
67	1	Power	VDD_DDR	Digital Power supply (1.8V)
159	1	Power	VDDQ_DDR	Digital Power supply (1.8V)
13, 20, 36, 50, 84, 96, 102, 114, 121, 125, 130, 131, 158 28, 29, 68, 107, 108	18	Ground	AVSS & DGND	Analog Ground and Digital Ground
Thermal Exposed Pad		Ground		Connect to ground plane through thermal via

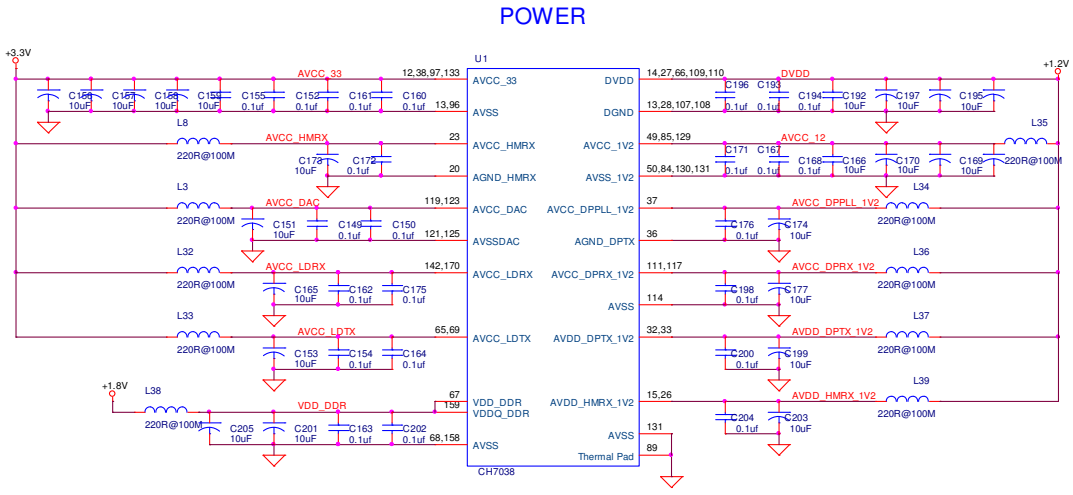

Figure 1: Power Supply Decoupling and Distribution

Note: All the Ferrite Beads described in this document are recommended to have an impedance of less than 0.3 Ω at DC and 220 Ω at 100MHz. Please refer to Walsin WB201209B221 for details or an equivalent part can be used for the diagram.

2.2 Power On Sequence and Reset

RSTB pin is the chip reset pin of CH7038/9. CH7038/9 will be reset when this pin is low. A power reset switch can be placed on the RSTB pin on the PCB as hardware reset for CH7038/9 as shown in **Figure 5**. When the pin is high, the reset function can also be controlled through the serial port.

Power On and Reset

There are two reset methods. One is RC reset. The power supply should be valid and stable for at least 9ms before RSTB becomes invalid as shown in **Figure 2**. A 1 MΩ and 0.1uF RC reset circuit is recommended.

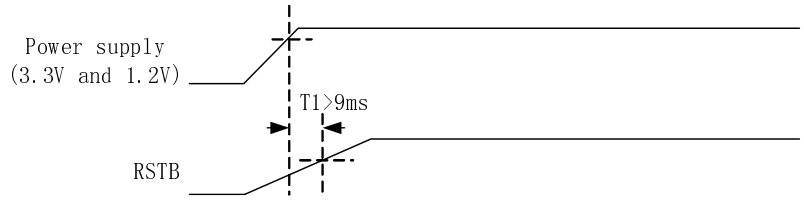

Figure 2: Power on and reset timing of RC

Another method is using an external reset signal. In this case, the power supply should be valid and stable for at least 9ms before the reset signal is valid. The pulse width of valid reset signal should be at least 100us. The timing is shown in **Figure 3.**

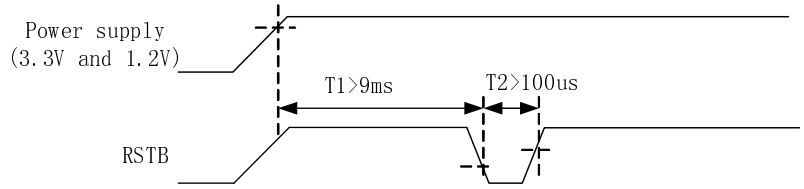

Figure 3: Power on and reset timing of external reset

Note: 1. The power supply will be valid when it rises to 90% of standard level.
2. The rising time (10%~90%) of power supply shall not exceed 2.5ms.
3. 1.2V shall be valid not later than 3.3V.
4. The rising threshold of RSTB is 2.4V.
5. The falling threshold of RSTB is 0.4V.

Reset and CH7038/9 State
After the reset operation of CH7038/9 is finished, CH7038/9 need maxim 308.65ms time to load firmware in flash and EEPROM. During firmware loading, CH7038/9 should be not accessed by external interface. The timing is shown in **Figure 4.**

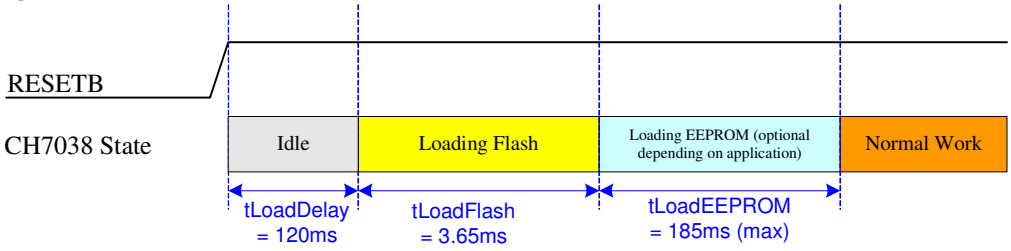

Figure 4: Reset and CH7038/9 State

2.3 Basic and Clock Pins

ATPG
The RESERVED pin (Pin134) is an internal test pin, should be pulled low through a 10 KΩ resistor.

• ISET

ISET pin sets the basic current. A 1 KΩ, 1% tolerance resistor should be connected between this pin and Ground plane using short and wide traces and a ground via as shown in **Figure 5.**

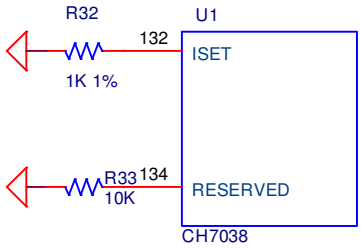

Figure 5: ISET pin and RESERVED Pin134

• XI and XO

CH7038/9 needs a 27M crystal to generate a reference clock.

The crystal load capacitance, C_L, is usually specified in the crystal spec from the vendor. As an example to show the load capacitors, **Figure 6** gives a reference design for crystal circuit design.

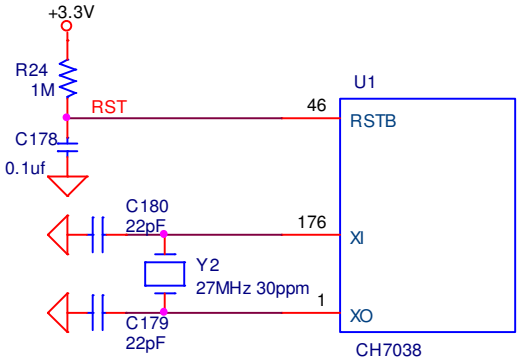

Figure 6: General Control Pins

• Reference Crystal Oscillator

CH7038/9 includes an oscillator circuit that allows a predefined-frequency crystal to be connected directly. Alternatively, an externally generated clock source may be supplied to CH7038/9. If an external clock source is used, it should have CMOS level specifications. The clock should be connected to the XI pin, and the XO pin should be left open. The external source must exhibit ±100 ppm or better frequency accuracy, and have low jitter characteristics.

If a crystal is used, the designer should ensure that the following conditions are met:

The crystal is specified to be predefined-frequency, ±100 ppm fundamental type and in parallel resonance (NOT series resonance). The crystal should also have a load capacitance equal to its specified value (C_L).

External load capacitors have their ground connection very close to CH7038/9 (C_{ext}).

To be able to tune, a variable capacitor may be connected from XI to ground.

Note that the XI and XO pins each has approximately 10 pF (C_{int}) of shunt capacitance internal to the device. To calculate the proper external load capacitance to be added to the XI and XO pins, the following calculation should be used:

$\mathbf{C}_{ext} = (2 \times C_L) - C_{int} - 2C_S$

Where
C_{ext} = external load capacitance required on XI and XO pins.
C_L = crystal load capacitance specified by crystal manufacturer.

C_{int} = capacitance internal to CH7038/9 (approximately 10-15 pF on each of XI and XO pins).
C_S = stray capacitance of the circuit (i.e. routing capacitance on the PCB, associated capacitance of crystal holder from pin to pin etc.).

In general,
$C_{int}XI = C_{int}XO = C_{int}$
$C_{ext}XI = C_{ext}XO = C_{ext}$

such that $C_L = (C_{int} + C_{ext}) / 2 + C_S$ and $C_{ext} = 2 (C_L - C_S) - C_{int} = 2C_L - (2C_S + C_{int})$

Therefore C_L must be specified greater than $C_{int} /2 + C_S$ in order to select C_{ext} properly.

After C_L (crystal load capacitance) is properly selected, care should be taken to make sure the crystal is not operating in an excessive drive level specified by the crystal manufacturer. Otherwise, the crystal will age quickly and that in turn will affect the operating frequency of the crystal.

For detail considerations of crystal oscillator design, please refer to **AN-06**.

2.4 General Control Pins

CH7038/9 has 8 general programmable IO pins, I2C, SPI and UART serial port. Following is a default pin map.

Table 2: GPIO Default Pinmap

Pin Name	Pin Number	Default function	Second function
GPIO0	135	GPIO (Button or switch)	I2S_D3 /SPI_SLAVE_CSB
GPIO1	2	UART_RX	GPIO
GPIO2	45	UART_TX	GPIO
GPIO3	90	GPIO (Button or switch)	CPU IF TE
GPIO4	118	GPIO (Button or switch)	I2S_D1
GPIO5	128	GPIO (Button or switch)	I2S_D2
GPIO6	40	VGA_HS	GPIO
GPIO7	39	VGA_VS	GPIO
LVDSCG3	6	GPI (switch: LVDS RX Single/Dual port) (note1)	
LVDSCG2	7	GPI (switch: LVDS RX OpenLDI/SPWG) (note1)	
DDC_SD_LDTX	47		SPI_HOST_DIN
DDC_SC_LDTX	48		SPI_HOST_DOUT
SPDM	88	SPDM (I2C master)	SPI_HOST_CSB
SPCM	89	SPCM (I2C master)	SPI_HOST_CLK
GPIO0	135	GPIO	SPI_SLAVE_CSB
ENA_BKL_LDRX	172		SPI_SLAVE_CLK
ENA_VDD_LDRX	173		SPI_SLAVE_DIN
IRQ	4	Infrared LED input	SPI_SLAVE_DOUT
SPD	94	(I2C slave)	
SPC	93	(I2C slave)	

Note1: If PIN140 (DDC_SC_HMTX) and PIN141 (DDC_SD_HMTX) are used, LVDSSG2 and LVDSSG3 can't be used as input.

2.4.1 GPIO Pins

CH7038/9 has eight GPIO pins. All GPIO pins can be configured as input or output. Some pins have multiplex

function. GPIO0, GPIO3, GPIO4, GPIO5 are recommended for normal application.

2.4.2 I2C serial port

• SPC, SPD and AS

SPD and SPC function as a slave I2C serial interface. The test points, which are connected to the SPD and SPC, are convenient for debug or update firmware. In the reference design, SPD and SPC pins are pulled up to 3.3V with 6.8 KΩ resistors as shown in **Figure 7**. AS pin is I2C address selection pin. A 10K pull-high resistor is used to set default I2C address.

• SPCM and SPDM

SPDM and SPCM are used to interface with an external EEPROM. SPDM and SPCM pins should be pulled up to 3.3V with 6.8 KΩ resistors as shown in **Figure 7**. The EEPROM can be used to store firmware and OSD information.

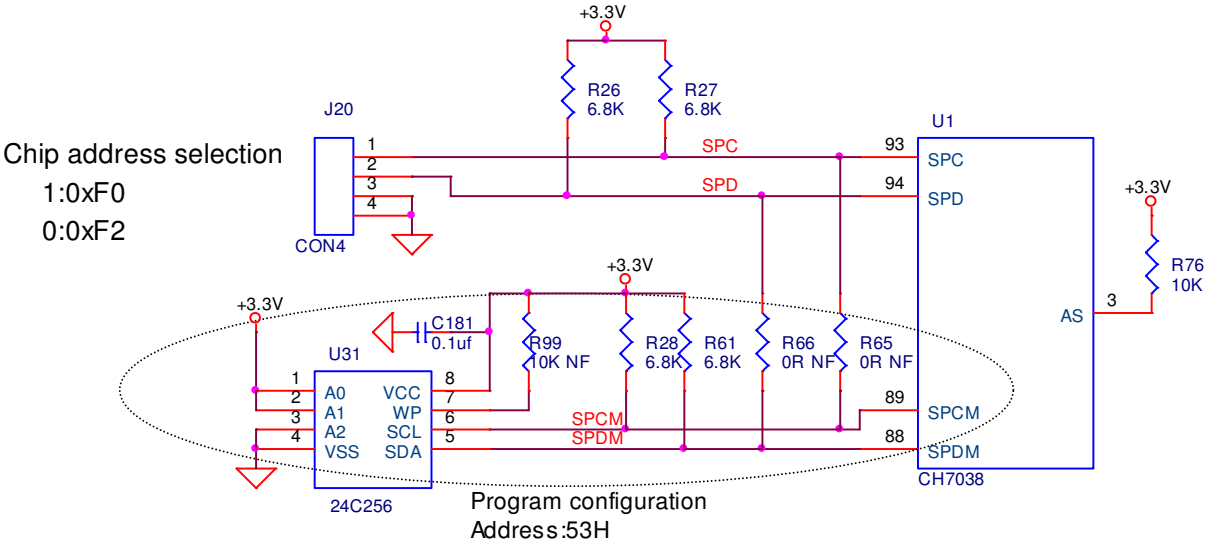

Figure 7: Serial Port Interface of CH7038/9

2.4.3 SPI Interface

CH7038/9 has one SPI master interface and one slave interface.

• SPI Master Interface
The SPI master interface can be used to interface with an external SPI flash or an external SPI device. Because these pins are multiplexed with I2C pins, all pins should be pulled up by a 6.8K resistor.

• SPI Slave Interface
The SPI slave interface of CH7038/9 is used as video data port. The internal DDR memory can be accessed by the interface.

2.4.4 UART Interface

CH7038/9 has one UART interface. The UART_RX and UART_TX can be connected to external SOC or MCU as control port for CH7038/9.

2.5 Audio Interface

CH7038/9 has two audio interfaces. Both interfaces can be configured to input or output interface. The audio interface of CH7038/9 can be configured as I2S or SPDIF interface. Following is a default pin map table.

Table 3: Audio Default Pin Map

Pin Name	Pin Number	Default function	Second function
I2S_WS	41	WS (I2S Input)	
I2S_DAT/SPDIF	42	DAT (I2S Input)	SPDIF in
I2S_CLK	43	CLK (I2S Input)	
I2S_MCLK	44	MCLK (I2S Input)	
I2S_WS	136	WS (I2S Output)	
I2S_DAT/SPDIF	137	DAT (I2S Output)	SPDIF out
I2S_CLK	138	CLK (I2S Output)	
I2S_MCLK	139	MCLK (I2S Output)	

• SPDIF Input Interface

When one audio interface is configured as SPDIF input interface, the input pin of SPDIF signal is the multi-function pin I2S_DAT/I2S_SPDIF.

The SPDIF signal has two voltage levels, so there are two input ways for CH7038/9. If SPDIF signal from audio codec is COMS or TTL level (3.3V~5V), it can be connected to the CH7038/9 directly. If SPDIF signal is COAX level (0.5V~1V), a voltage level shifting is required as shown in **Figure 8**.

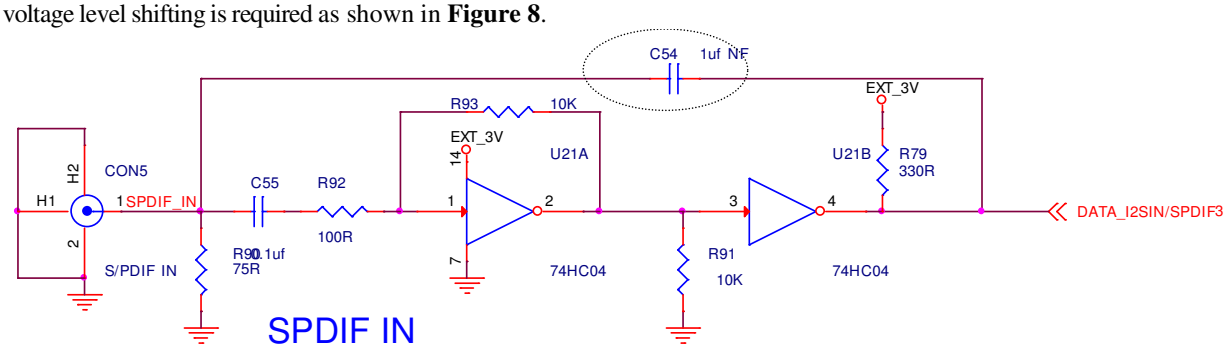

Figure 8: SPDIF Level Shift

• I2S Input Interface

For I2S input interface, the I2S bus consists of four serial bus lines: a line with data channel [DAT], a word select line [WS], and a clock line [CLK] and an optional clock line [MCLK].

• SPDIF Output Interface

For SPDIF output interface, the output pin of SPDIF signal is the multi-function pin I2S_DAT/I2S_SPDIF.

The SPDIF signal has two voltage levels, so there are two output ways for CH7038/9. If COMS or TTL level (3.3V~5V) of SPDIF signal is required, it can be connected to the CH7038/9 directly. If COAX level (0.5V~1V) of SPDIF signal is required, a resistor divider is needed as shown in **Figure 9**.

• I2S Output Interface

For I2S output interface, the I2S bus consists of four serial bus lines: a line with data channel [DAT], a word select line [WS], a clock line [CLK], and an optional clock line [MCLK]. Refer to **Figure 9** for the design example which uses I2S to interface an audio codec.

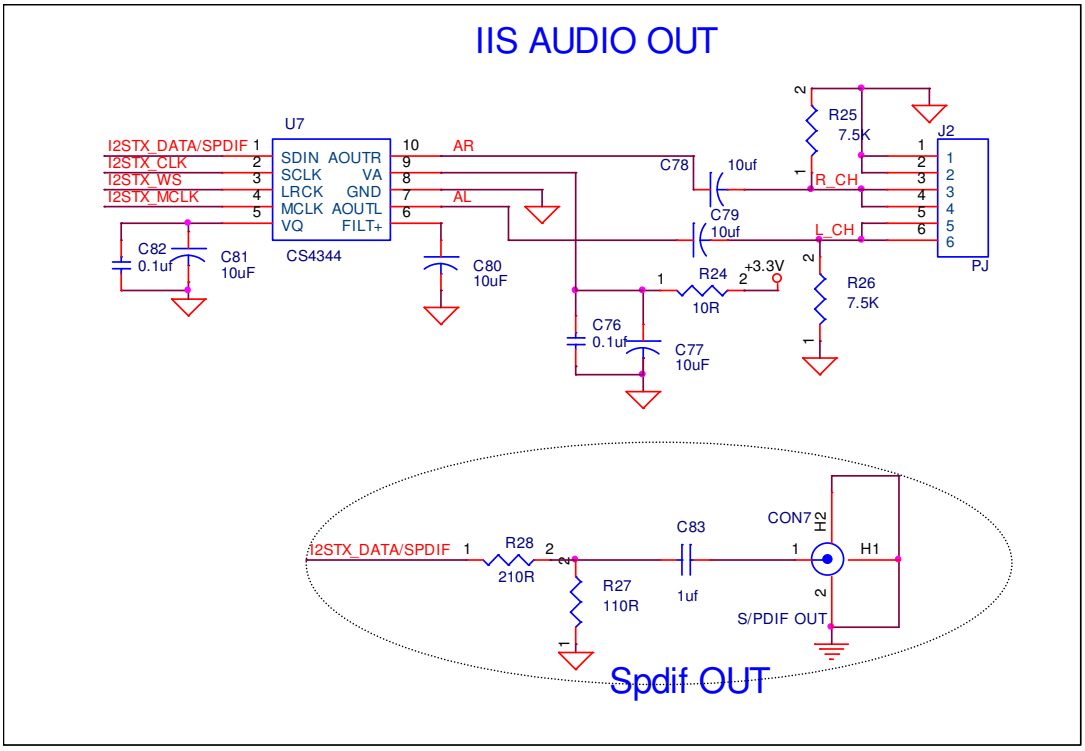

Figure 9: CH7038/9 SPDIF and IIS Output

2.6 TTL Interface

CH7038/9 can support multi-format TTL output and input. The voltage level of TTL signal can be 1.8V or 3.3V by connecting the power supply of TTL signal to 1.8V or 3.3V.

• TTL Input Interface

The following table indicates the supported input data format and pin map by the CH7038/9.

Table 4: TTL Input PIN map

MULTI	Format	D[23:16]	D[15:8]	D[7:0]
0	RGB888	R[7:0]	G[7:0]	B[7:0]
	RGB666	2'b00,R[5:0]	2'b00,G[5:0]	2'b00,B[5:0]
	RGB565	3'b000,R[4:0]	2'b00,G[5:0]	3'b000,B[4:0]
	RGB555	3'b000,R[4:0]	3'b000,G[4:0]	3'b000,B[4:0]
	Special RGB	R[7:3],G[7:5]	R[2:0],G[1],G[4:2], B[7]	B[6:3],G[0],B[2:0]
	8bit 4:2:2 YCbCr	8'h00	Y[7:0]	C[7:0]
	10bit 4:2:2 YCbCr	4'h0, Y[9:6]	Y[5:0],C[9:8]	C[7:0]
	8bit 4:4:4 YCbCr	Y[7:0]	Cb[7:0]	Cr[7:0]
	Consecutive aligned 666 RGB input	6'h00, R[5:4]	R[3:0],G[5:2]	G[1:0],B[5:0]

		Consecutive aligned 565 RGB input	8'h00	R[4:0],G[5:3]	G[2:0],B[4:0]
		Consecutive aligned 555 RGB input	8'h00	1'b0, R[4:0],G[4:3]	G[2:0],B[4:0]
1	PA	0		4'h0, R[7:4]	R[3:0],G[7:4]
	PB			4'h0, G[3:0]	B[7:0]
	PA	1		7'h00, R[5]	R[4:0],G[5,3]
	PB			7'h00, G[2]	G[1:0],B[5:0]
	PA	2			R[4:0],G[5,3]
	PB				G[2:0],B[4:0]
	PA	3			1'b0,R[4:0],G[4,3]
	PB				G[2:0],B[4:0]
	PA	4		4'h0, R[7:4]	R[3],G[7:5],R[2:0],G[1]
	PB			4'h0, G[4:2], B [7]	B[6:3],G[0],B[2:0]
	PA	5			Y[7:0]
	PB				C[7:0]
	PA	6		6'h00, Y[9:8]	Y[7:0]
	PB			6'h00, C[9:8]	C[7:0]
	PA	7		4'h0, Y[7:4]	Y[3:0],Cb[7:4]
	PB			4'h0, Cb[3:0]	Cr[7:0]
2	PA	0			R[7:0]
	PB				G[7:0]
	PC				B[7:0]
	PA	7			Y[7:0]
	PB				Cb[7:0]
	PC				Cr[7:0]
BT1120 8bit				Cb/Cr[7:0]	Y[7:0]

Note: PA, PB, PC represent the parts of one pixel data.

• TTL Output Interface

Following table is a default pin map table of CH7038/9 TTL output. For detailed TTL output format, please refer to the CH7038/9 datasheet.

Table 5: TTL Output PIN map

Format			**D[23:16]**	**D[15:8]**	**D[7:0]**
SDR		RGB888	R[7:0]	G[7:0]	B[7:0]
		RGB666	2'b00,R[5:0]	2'b00,G[5:0]	2'b00,B[5:0]
		8bit 4:2:2 YCbCr	8'h00	C[7:0]	Y[7:0]
		8bit 4:4:4 YCbCr	Cr[7:0]	Y[7:0]	Cb[7:0]
2x Multiplexed	PA	24bit-RGB mode0		4'h0, R[3:0]	G[3:0], B[7:4]
	PB			4'h0, R[7:4]	G[7:4], B[7:4]
	PA	24bit-		4'h0, Cr[3:0]	Y[3:0], Cb[3:0]

	PB	YCbCr4:4:4 mode0		4'h0, Cr[7:4]	Y[7:4], Cb[7:4]
	PA	18bit-RGB Mode0		7'h00, R[2]	R[1:0], G[2,0], B[2,0]
	PB			7'h00, R[5]	R[4:3], G[5,3], B[5,3]
	PA	18bit-YCbCr4:4:4 mode0		7'h00, Cr[2]	Cr[1:0], Y[2,0], Cb[2,0]
	PB			7'h00, Cr[5]	Cr[4:3], Y[5,3], Cb[5,3]
	PA	YCbCr4:2:2			Y[3:0], C[3:0]
	PB				Y[7:4], C[7:4]
	PA	BT656/ BT1120 Like format			C[7:0]
	PB				Y[7:0]
3x Multiplexed	PA	24bit-RGB			R[7:0]
	PB				G[7:0]
	PC				B[7:0]
	PA	YCbCr4:4:4			Cr[7:0]
	PB				Y[7:0]
	PC				Cb[7:0]
24bit DDR	EA	24bit-RGB	RE[7:0]	GE[7:0]	BE[7:0]
	EB		RO[7:0]	GO[7:0]	BO[7:0]
18bit DDR	EA	18bit-RGB	6'h00, RE[5:4]	RE[3:0], GE[5:2]	GE[1:0], BE[5:0]
	EB		6'h00, RO[5:4]	RO[3:0], GO[5:2]	GO[1:0], BO[5:0]
16bit DDR	EA	16bit-YCbCr4:2:2		Cb[7:0]	Y[7:0]
	EB			Cr[7:0]	Y[7:0]
12bit DDR	EA	24bit-RGB Mode0		4'h0, G[3:0]	B[7:0]
	EB			4'h0, R[7:4]	R[3:0], G[7:4]
	EA	24bit YCbCr4:4:4		4'h0, Y[3:0]	Cb[7:0]
	EB			4'h0, Cr[7:4]	Cr[3:0], Y[7:4]
9bit DDR	EA	18bit-RGB Mode0		7'h00, G[2]	G[1:0], B[5,0]
	EB			7'h00, R[5]	R[4:0], G[5,3]
	EA	18bit YCbCr4:4:4		7'h00, Y[2]	Y[1:0], Cb[5,0]
	EB			7'h00, Cr[5]	Cr[4:0], Y[5,3]
8bit DDR	EA	YCbCr4:2:2			Y[7:0]
	EB				Cb[7:0]/Cr[7:0]
BT1120		8bit		Cb/Cr[7:0]	Y[7:0]
		10bit	D[15:8], D[19:18]<->Y[9:0] | D[7:0], D[17:16] <->Cb/Cr[9:0]		

2.7 LVDS Interface

CH7038/9 can support one or two lane LVDS output and input.

2.7.1 LVDS Input Interface

LVDS input is shown in **Figure 10**.

CH7038/9 can accept 18bit or 24bit SPWG/OpenLDI format data from LVDS transmitter. If video signals come from

single port, PortR is used as input interface.

CH7038/9 LVDS input channel differential pairs have Optional Internal termination resistors of 100Ω inside. It has the advantage of terminating as close as possible to the receiver (minimizing stubs) and also saving board space and reducing component count.

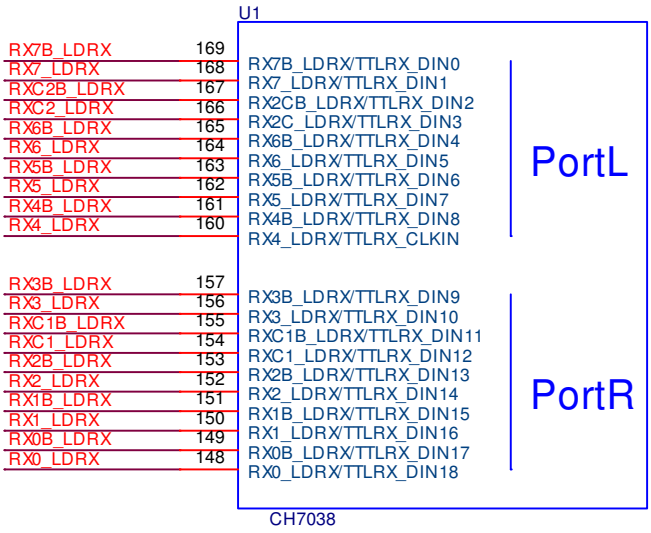

Figure 10: CH7038/9 LVDS Input Pins

2.7.2 LVDS Onput Interface

LVDS output is shown in **Figure 11**.

CH7038/9 can be configured as 18bit or 24bit SPWG/OpenLDI format data. The LVDS TX pin order and polarity can be configured by register. If only one single port is required, PortR is used as the output interface.

In order to facilitate LVDS loop test, the following pin pairs are swapped by firmware default configuration.

TXC1/TXC1B<-> TX3/TX3B
TXC2/TXC2B<-> TX7/TX7B

SD_LDTX, SC_LDTX can be used to read LVDS panel EDID. These two signals should be pulled up by 6.8K~10K resistors.

ENPWR_LDTX, ENABLK_LDTX, PWM_LDTX are used to control LVDS power and backlight as shown in **Figure 12**.

If CH7038/9 is used in application of 3D LVDS output, please contact Chrontel Application Group for more information.

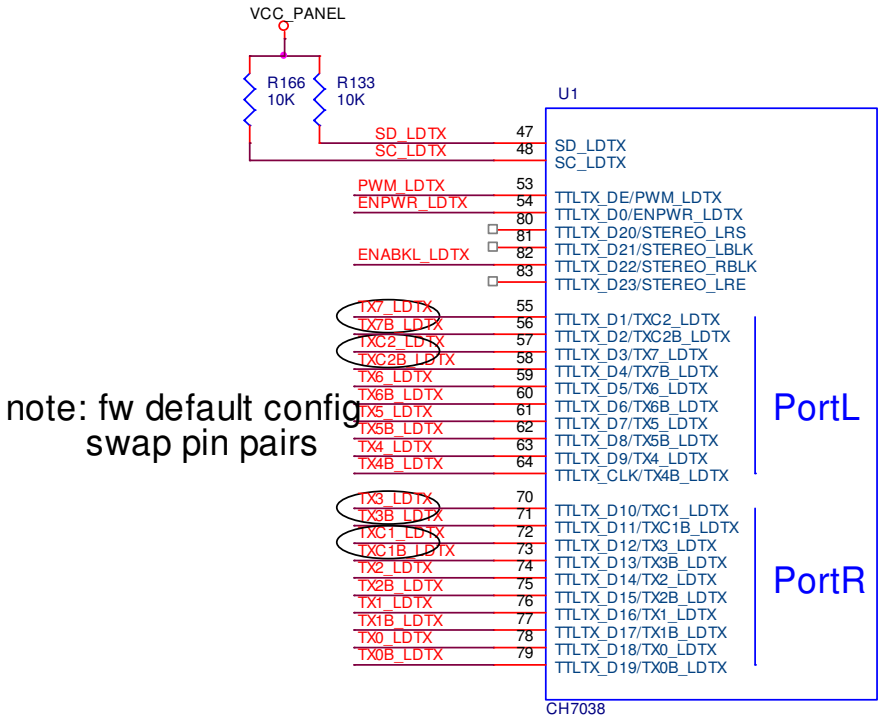

Figure 11: CH7038/9 LVDS Output Pins

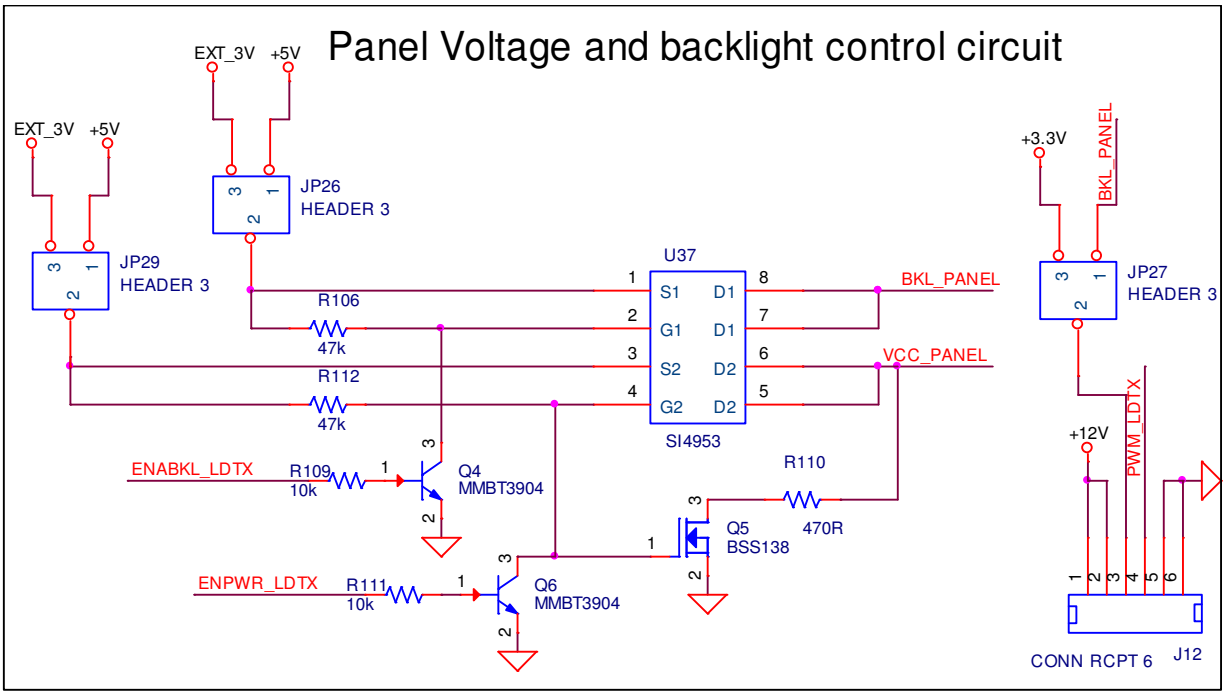

Figure 12: LVDS Panel Voltage and Backlight Control Circuit

2.7.3 LVDS Differential Trace Layout

Since LVDS signals are differential, they must be routed in differential pairs. The differential impedance of LVDS pairs should be 100Ω. It is recommended that 5 mils traces should be used in routing these signals. There should be 7 mils spacing between each intra pair.

The length for a pair of intra differential signals should be matched within 5 mils. The length for inter pairs should be matched within 100 mils.

Bend which is smaller than 45 degrees should be avoided.

The differential pairs should be placed above solid ground plane or power plane to minimize un-continued impedance.

Smallest size vias and connector pads are recommended to be used. It is recommended that 12 mils inner diameter and 18 mils outer diameter vias or smaller one should be used in routing these signals.

To maintain constant differential impedance along the length, it is important to keep the trace width and spacing uniform along the length, as well as maintain good symmetry between the two lines.

2.8 HDMI Interface

CH7038/9 has a HDMI input and a HDMI output interface.

2.8.1 HDMI Input Interface

HDMI input is shown in **Figure 13**.

• RXC/RXCB, RX0/RX0B, RX1/RX1B and RX2/RX2B

Those four pair signals of HDMI RX are high frequency differential pairs, and should be routed by precaution. Please refer to the **section 2.9.4** for layout guide.

• HPD_HMRX

This output pin connects to the +5V power through a 1KΩ resistor. Refer to **Figure 13** for the design example.

•DDC_SD_HMRX and DDC_SC_HMRX

DDC_SD_HMRX and DDC_SC_HMRX are used to interface with the DDC of HDMI source. The DDC is used by CH7038/9 to tell source the capabilities and characteristics of the CH7038/9 by transfer the E-EDID data. This DDC pair needs to be pulled up to 5V through 47K resistors and diodes as shown in **Figure 13**. The diode is used to avoid back drive from DDC signal.

Note: Because HDMI source has internal 5V pull-up resistors on DDC trace. In order to avoid back drive, the power for DDC circuit of CH7038/9 should be independent 5V power supply. Using a diode with low forward voltage is another option. It is better that the forward voltage of the diode does not exceed 0.3V to avoid the voltage on pull-up resistors drops too low.

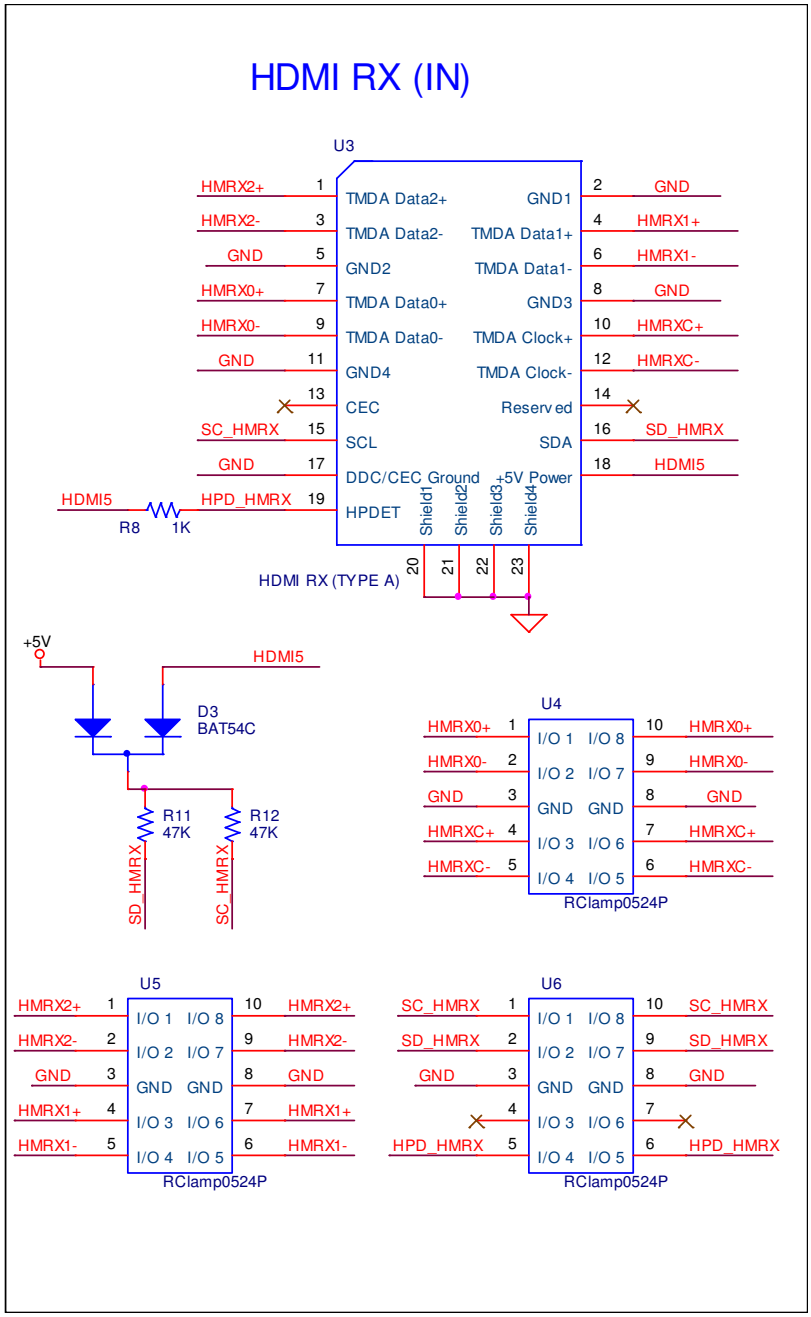

Figure 13: HDMI Outputs with ESD Protection

2.8.2 HDMI Output Interface

HDMI output is shown in **Figure 14**.

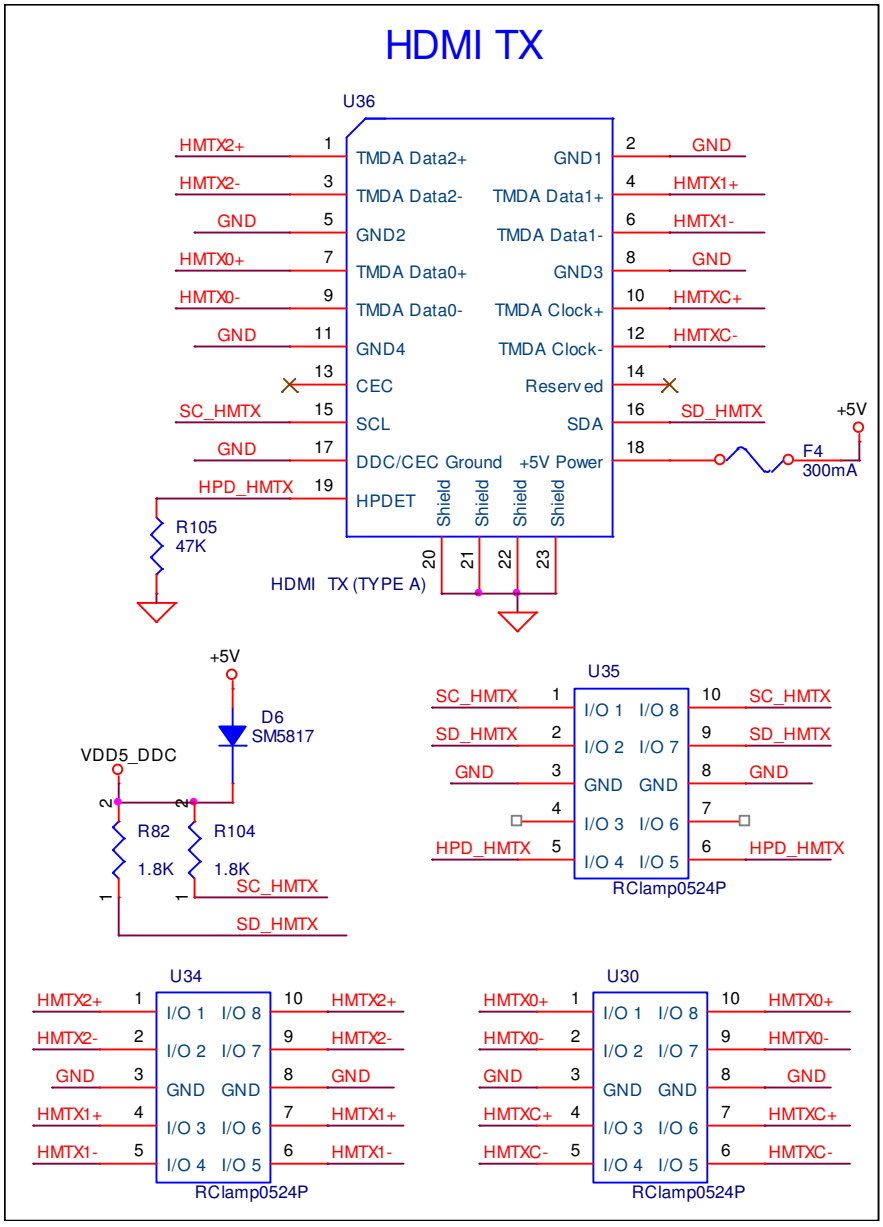

Figure 14: HDMI Input with ESD Protection

• TXC/TXCB, TX0/TX0B, TX1/TX1B and TX2/TX2B

Those four pair signals of HDMI TX are high frequency differential pairs, and should be routed by precaution. Please refer to the **section 2.9.4** for layout guide.

• HPD_HMTX

This input pin should be pull down to GND through a 47KΩ resistor. Refer to **Figure 14** for the design example.

•DDC_SD_HMTX and DDC_SC_HMTX

DDC_SD_HMTX and DDC_SC_HMTX are used to interface with the DDC of HDMI source. The DDC is used by CH7038/9 to read the capabilities and characteristics of the HDMI sink by transfer the E-EDID data. This DDC pair needs to be pulled up to 5V through 1.8K resistors and diodes as shown in **Figure 14**. The diode is used to avoid back drive from DDC signal.

Note: Because HDMI source have internal 5V pull-up resistors on DDC trace. In order to avoid back drive, the power for DDC circuit of CH7038/9 should be independent 5V power supply. Using a diode with low forward voltage is another option. It is better that the forward voltage of the diode does not exceed 0.3V to avoid the voltage on pull-up resistors drops too low.

2.8.3 ESD Protection for HDMI Interface

In order to minimize the hazard of ESD, a set of protection diodes are highly recommended for each HDMI Outputs (data and clock).

International standard EN 55024:1998 establishes 4kV as the common immunity requirement for contact discharges in electronic systems. 8kV is also established as the common immunity requirement for air discharges in electronic systems. International standard EN 61000-4-2:1995 / IEC 1000-4-2:1995 establishes the immunity testing and measurement techniques.

System level ESD testing to International standard EN 61000-4-2:1995 / IEC 1000-4-2:1995 has confirmed that the proper implementation of Chrontel's recommended diode protection circuitry, using SEMTECH Rclamp0524P diode array devices, will protect the CH7038/9 device from HDMI panel discharges of greater than 8kV (contact) and 16kV (air). The RClampTM0524P have a typical capacitance of only 0.30pF between I/O pins. This low capacitance won't bring too much bad effect on HDMI eye diagram test.

2.8.4 HDMI Differential Trace Layout

2.9.4.1 Differential Pair Impedance

HDMI signal have four high frequency differential pairs. For HDMI input, those differential pairs are RXC/RXCB, RX0/RX0B, RX1/RX1B and RX2/RX2B. For HDMI output, those differential pairs are TXC/TXCB, TX0/TX0B, TX1/TX1B and TX2/TX2B.

To match the external cable impedance and maintain the maximal energy efficiency it is important that those high frequency differential pairs of HDMI meet the impedance target of 100 Ω ± 10% for the differential data/clock traces. The restriction of this impedance target is to prevent any loss of signal strengths resulting from a reflection of unwanted signals. The impedance can be acquired by proper design of trace length, trace width, signal layer thickness, board dielectric, etc. It is recommended that 5 mils traces should be used in routing these signals. There should be 7 mils spacing between each intra pair.

The differential pairs should be placed above solid ground plane or power plane to minimize un-continued impedance.

Use the smallest size vias and connector pads. It is recommended that 12 mils inner diameter and 18 mils outer diameter vias or smaller one should be used in routing these signals. At most one via can be used on trace.

2.9.4.2 Trace Routing Length

To prevent from capacitive and impedance loading, trace lengths should be kept as minimal as possible. Vias and bends should always be minimized; inductive effects may be introduced, causing spikes in the signals. Trace routing lengths from CH7038/9 to the HDMI/DVI connector are limited to a maximum of 2 inches. The CH7038/9 should be as close to the HDMI/DVI connector as possible.

2.9.4.3 Length Matching for Differential Pairs

The HDMI/DVI specifies the intra-pair skew and the inter-pair skew as in **Table 6**. The intra-pair skew is the maximum allowable time difference on both low-to-high and high-to-low transitions between the true and complement signals. The inter-pair skew is the maximum allowable time difference on both low-to-high and high-to-low transitions between any two single-ended data signals that do not constitute a differential pair.

Table 6: Maximum Skews for the HDMI/DVI Transmitter

Skew Type	Maximum at Transmitter
Intra-Pair Skew	0.15 T_{bit}
Inter-Pair Skew	0.20 T_{Pixel}

Where T_{bit} is defined as the reciprocal of Data Transfer Rate, and T_{Pixel} is defined as the reciprocal of Clock Rate.

Therefore, T_{Pixel} is 10 times T_{bit}. In other words, the intra-pair length matching is much more stringent than the inter-pair length matching.

It is recommended that length matching of both signals of a differential pair be within 5 mils. Length matching should occur on a segment by segment basis. Segments might include the path between vias, resistor pads, capacitor pads, a pin, an edge-finger pad, or any combinations of them, etc. Length matching from one pair to any other should be within 100 mils.

Note that lengths should only be counted to the pins or pad edge. Additional etch within the edge-finger pad, for instance, is electrically considered part of the pad itself.

2.9 DisplayPort Interface

CH7038/9 has DP/eDP input and DP/eDP output interface.

2.9.1 DP/eDP Input

• RX_DP0P/N, RX_DP1P/N

These pins accept two AC-coupled differential pair signals from the DisplayPort transmitter. Since these pair signal traces may be toggled at speeds up to 2.7 GHz, should be routed by precaution. Please refer to the **section 2.9.4** for layout guide.

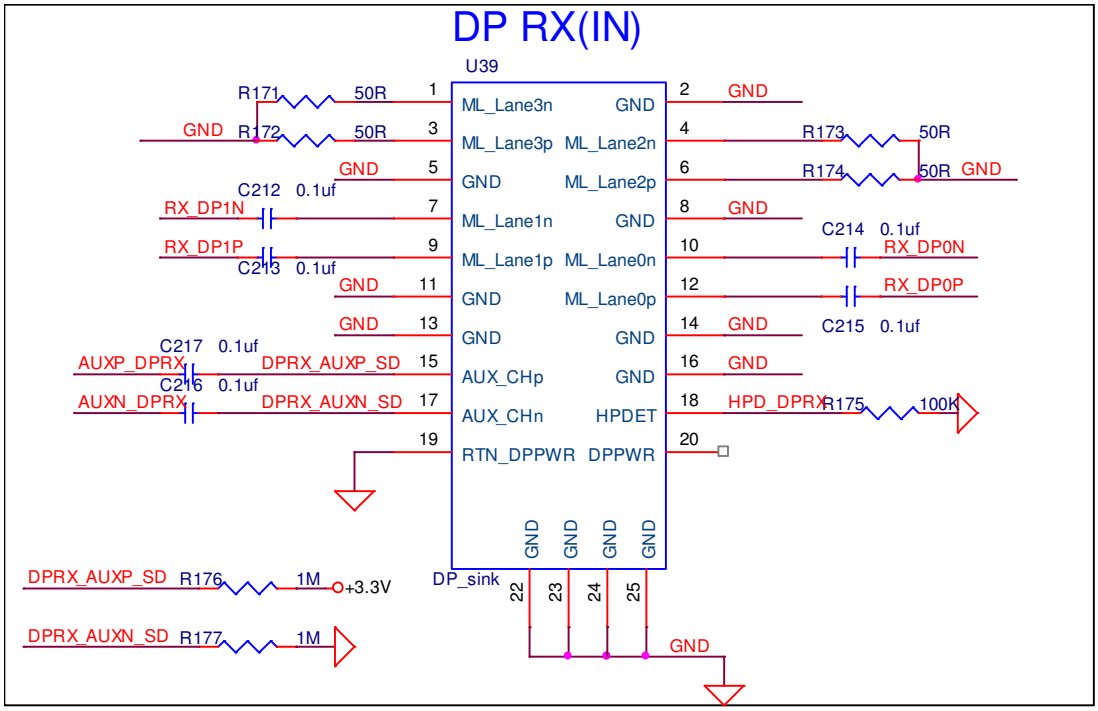

Figure 15: CH7038/9 DP Inputs

• AUXP_DPRX and AUXN_DPRX

These two pins are DisplayPort AUX channel control that accepts a half-duplex, bi-directional AC-coupled differential signal.

They must have the AC-coupling capacitors, and 100nF capacitors are recommended in this document, as shown in **Figure 15**.

• HPD_DPRX

This output pin indicates whether CH7038/9 is active or not. It also generates interrupt pulse as defined by DisplayPort standard. Output voltage is 3.3V. A resistor more than 100K-Ohm should be connected between this pin and GND, as shown in **Figure 15**.

2.9.2 DP/eDP Output

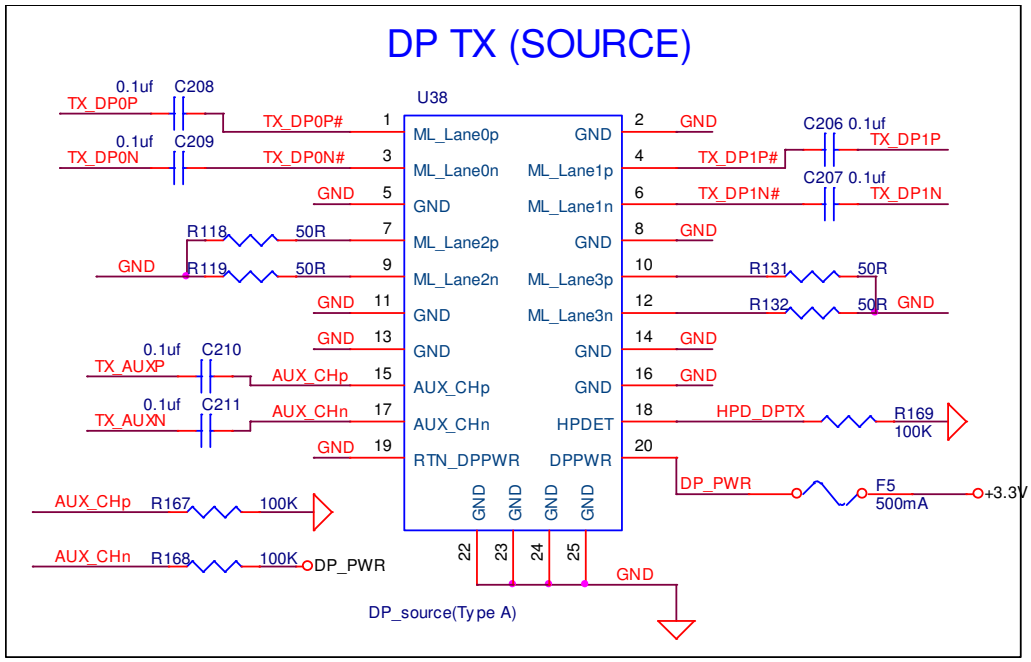

Figure 16: CH7038/9 DP Outputs

• TX_DP0P/N, TX_DP1P/N

These pins transmit two AC-coupled differential pair signals to the DisplayPort sink. Please refer to the **section 2.10.3** for layout guide.

• TX_AUXP and TX_AUXN

These two pins are DisplayPort AUX channel control that accepts a half-duplex, bi-directional AC-coupled differential signal.

They must have the AC-coupling capacitors, and 100nF capacitors are recommended in this document, as shown in **Figure 16**.

• HPD_DPTX

This input pin indicates whether DP sink is active or not. A resistor more than 100K-Ohm should be connected between this pin and GND, as shown in **Figure 16**. If DP TX of CH7038 will be connected with external DP monitor, a circuit should be added to avoid back drive from monitor. For detail circuit, please refer the reference schematic.

2.9.3 DP differential pair signals layout

DP signal have two high frequency differential pairs. It is strongly recommended that the connection of these video signals between the DP connector, source or sink and the CH7038/9 should be kept as short as possible.

To match the external cable impedance and maintain the maximal energy efficiency it is important that those high frequency differential pairs of DP meet the impedance target of 100 Ω ± 10% for the differential data/clock traces.

It is recommended that 5 mils traces should be used in routing these signals. There should be 7 mils spacing between each intra pair.

The length for a pair of intra differential signals should be matched within 5 mils. The length for inter pairs should be matched within 2 inches.

Bend which is smaller than 45 degrees should be avoided.

The AC coupling capacitors for the differential signals should be placed close to CH7038/9.

The differential pairs should be placed above solid ground plane or power plane to minimize un-continued impedance.

Use the smallest size vias and connector pads. It is recommended that 12 mils inner diameter and 18 mils outer diameter vias or smaller one should be used in routing these signals. At most one via can be used on trace.

These differential pairs should be isolated as much as possible from the analog outputs and analog circuitry. For optimum performance, these signals should not overlay the analog power or analog output signals.

2.10 DAC Output Pins

CH7038/9 has three separate 9-bit video DACs. Corresponding to three DACs, CH7038/9 has three DAC output pin, DAC0, DAC1 and DAC2. An internal analog switch can switch DAC0 signal to DAC0 pin or CVBS pin.

2.10.1 VGA Output

• RDAC, GDAC and BDAC

Three on-chip 9-bit high speed DACs provide RGB output. If the DACs require double termination, a 75 Ω resistor should be placed between each DAC pin and the ground, as shown in **Figure 17**.

• HSO and VSO

The HSO and VSO are COMS output Pins, The voltage level is the same with AVCC.

• VGA_DDC_SC and VGA_DDC_SD

VGA_SCL and VGA_SDA are used to interface with the DDC of VGA monitor. This DDC pair needs to be pulled up to 5V through 1.8K resistors as shown in **Figure 17**. A low instantaneous forward voltage diode is used to avoid back drive current from VGA monitor.

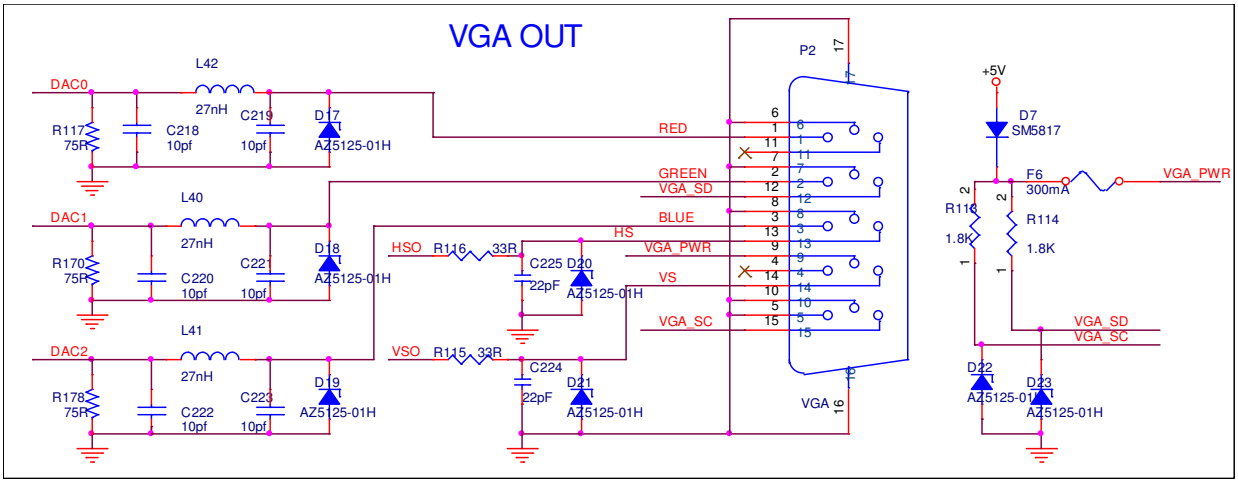

Figure 17: The CH7038/9 VGA Outputs

2.10.2 CVBS Output

The CVBS signal is analog video signal which come from DAC0. A 75Ω resistor should be placed between DAC0 pin and the ground as shown in **Figure 18**. A low pass filter is used to improve the quality of CVBS signal.

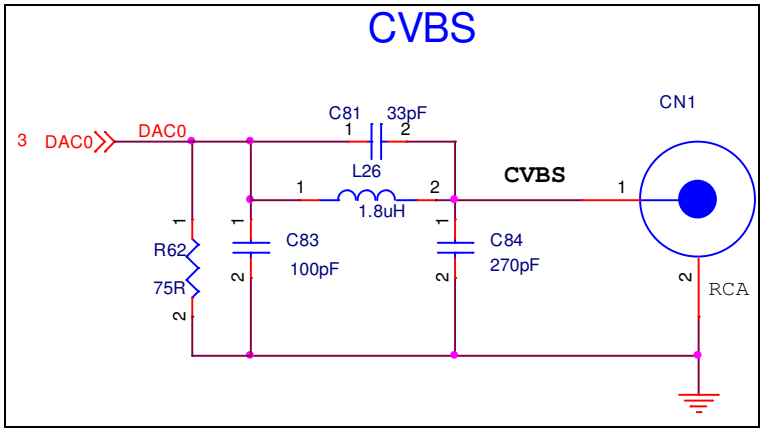

Figure 18: CH7038/9 CVBS output

2.10.3 S-Video Output

The S-Video signals include Y and C components come from DAC1 and DAC2 separately. A 75 Ω resistor should be placed between DAC pin and the ground as shown in **Figure 19**. A low pass filter is used to improve the quality of S-video signal.

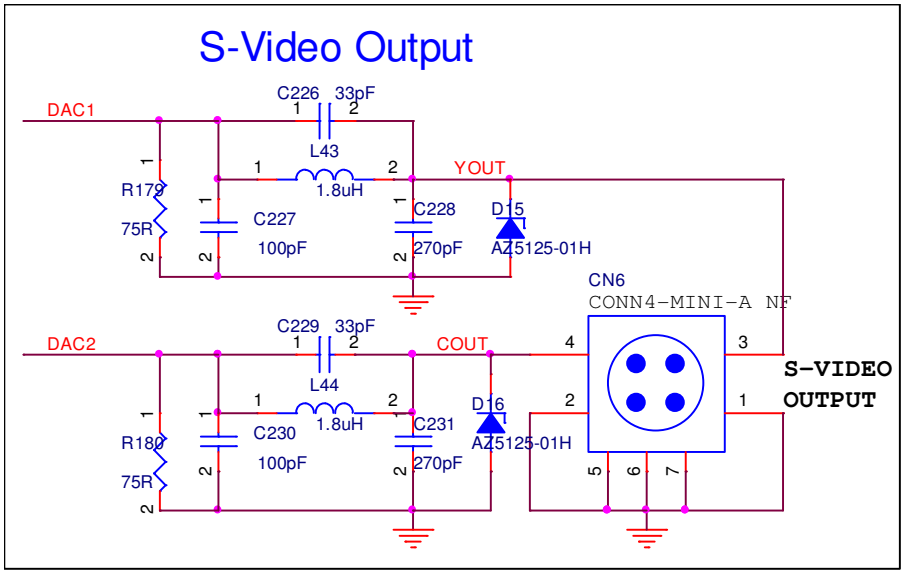

Figure 19: CH7038/9 S-Video outputs

2.10.4 Component YPbPr Output

The component signals include Y, Pb and Pr components come from DAC0, DAC1 and DAC2 separately. A 75 Ω resistor should be placed between DAC pin and the ground as shown in **Figure 20**. A low pass filter is used to improve the quality of YPbPr video signal.

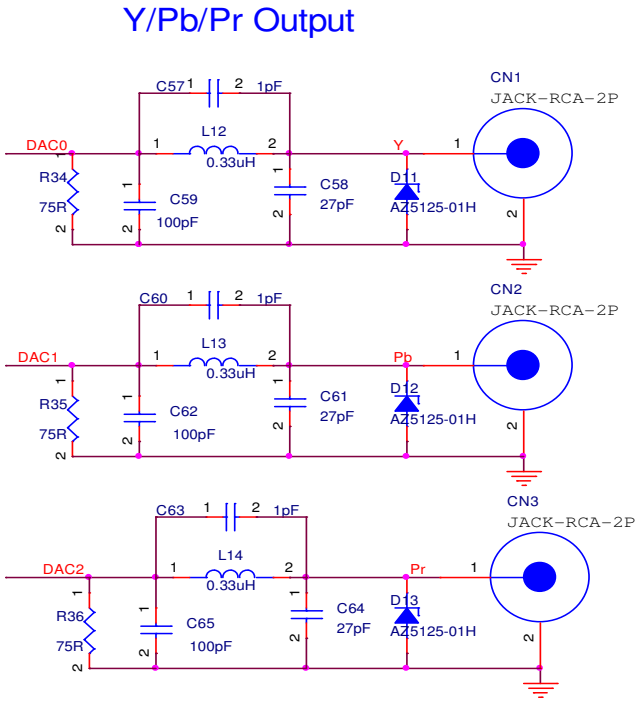

Figure 20: CH7038/9 YPbPr outputs

2.11 Thermal Exposed Pad Package

The 176-pin QFP package of CH7038/9 has a thermal exposed pad. The advantage of the thermal exposed pad package is that the heat can be dissipated through the ground layer of the PCB more efficiently.
For maximum heat dissipation, the exposed pad of the package should be soldered to the PCB. For PCB design, at least 4x4 ground vias should be placed on the thermal pad position to improve heat dissipation as shown in **Figure 21**.

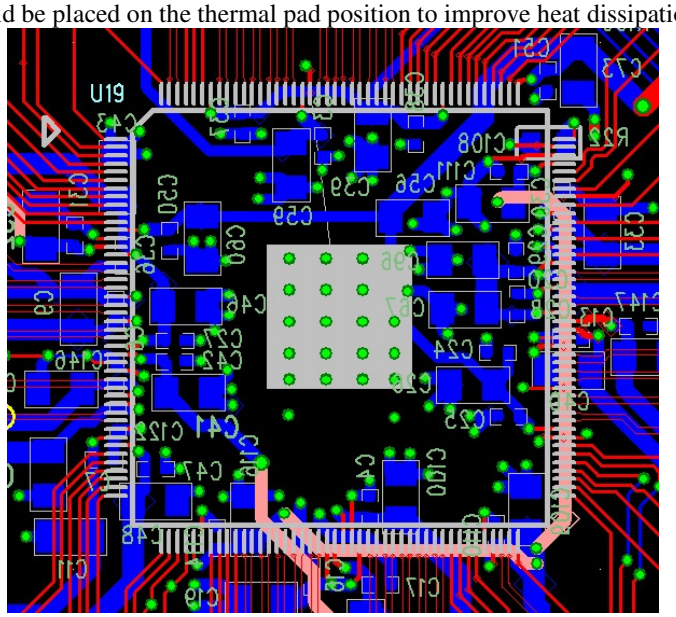

Figure 21: Exposed Pad amd Ground Vias

BTW, for the assembly process, it is important to limit the amount of solder paste that is put under the thermal pad. If too much paste is put on the PCB, the package may float during assembly. Compared with the solder mask of thermal pad, the paste mask should be shrank to70%~80%.

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